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Patentanmeldung Nr. Patent application No. Demande de brevet n°

04100427.6

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For the President of the European Patent Office

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R C van Dijk

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(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
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Latch circuit

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Latch circuit

The invention relates to a latch circuit.

Latch circuits are large-scale used circuits e.g. for memorizing a binary signal, for use in state machines, frequency dividers, counters. Modern technology trends are low-voltage supply for digital circuits for obtaining a relatively lower power consumption of logic families operating at lower and lower supply voltages and down-scaling of the oxide thickness for reliability reasons. When speed is an important feature, the design of digital building blocks may be inspired by analog techniques since any of the classical digital solutions working at low speed do not provide the required performance. The fastest logic family in MOS technology, which is widespread in modern integrated circuits, is the so-called Source Coupled Logic (SCL) family. However, at relatively low supply voltages e.g. 1.2 V or lower, SCL family does not work properly due to the stacking of transistors i.e. between a positive supply voltage and ground there are at least three transistors. This category includes AND, OR, XOR gates and the D-latch. The D-latch is relatively difficult function to be implemented because the requirements for a relatively small set-up and hold times are obtained with a relatively high power consumption. When working with signals having an equivalent period comparable with the time delay through the latch, the latch should take decisions i.e. to assert either logical 1 or logical 0 when receives a clock signal, and therefore a sufficient gain is necessary. However, the transconductance of modern MOS transistors is lower than their bipolar counterparts and therefore wider devices having higher currents for achieving the gain requirements, are necessary. As a consequence, the rise and fall times of the digital signals are deteriorated and therefore the speed.

US-2003/0001646 describes, among other circuits, a latch circuit as shown in Fig.6. Fig. shows the SCL triggered D-latch. When CK is positive, the differential pair M1, M2 tracks the input D and on the negative level of the CK the latch M3, M4 becomes active memorizing in a binary format the input signal provided at the D input. The following disadvantages are observed:

- the supply voltage is limited to $V_{GS}+2(V_{GS}-V_T)+\Delta V$ where V_{GS} is the gate-source voltage of one of the transistors M1...M4, or the MOS current source I_0, V_T is the

threshold voltage of the process and ΔV is the voltage drop on the resistor R or the resistor needed to bias the transistors M1 and M2. In modern processes like CMOS18 the supply voltage is limited to 1.8V and the circuit should work at 1.62V (1.8V-10%).

- the latch and the differential pair share the same load together. Therefore the latch has the difficult task to take decisions on a large capacitance load given by its own stray capacitances $(C_{GS}+C_{DS})/2$, the parasitic capacitances of M1 and M2 and the load capacitance given by wiring, fan-in and the resistor R. The use of a buffer between the latch and the gain stage is excluded due to the lack of voltage room and the lack of good source-followers in baseline digital processes.
- the intrinsic delay between the data path and the clock path. The clock path has a larger delay than the data path and therefore the delay times from CK to Q output ($t_{dCK->Q}$) and from D to Q output ($t_{dD->Q}$) are not equal. This can impair the function of a phase detector and can generate extra offset in a PLL loop in lock.

the fact that transistors are stacked we need a level shifter between the D level and the CK level asking for extra source followers or level shifters that decrease the speed of operation and enhance the intrinsic delay between the data path and the clock path. Hence, there is a need to obtain a latch operating at relatively high frequency and using relatively low supply voltages.

The invention is defined by the independent claims 1 and 10. The dependent claims define advantageous embodiments. It is provided a latch circuit comprising,

- a differential input with an inverting input and a non-inverting input,
- a differential output with an inverting output and a non-inverting output,
- one of said non-inverting outputs being coupled to one of said input, having opposite polarity; and
- a control input for receiving a control signal for determining a threshold for an input signal such that if the signal is at larger than the threshold the non-inverting is in a HIGH logic state and in a LOW state if the signal is smaller than the threshold, respectively.

Logical states of a logic circuit as a latch are determined inter alia by the supply voltage. It is defined a threshold level, which may be a current or a voltage, and a signal having a higher amplitude that the threshold level determines a logical 1 signal and a logical 0, otherwise. For a given family of logic circuits, the threshold level depends on the supply voltage. In order to adapt to a relatively large set of supply voltages i.e. between 3V and .9 V, a control signal, which determines the threshold level is provided. Furthermore, the

latch circuit is adapted to receive single ended signals and provides differential output signals.

It is also provided a latch circuit adapted for differential input signals and comprising a first latch portion and second latch portion, which are substantially identical, each latch portion comprising

- a differential input with an inverting input and a non-inverting input,
- a differential output with an inverting output and a non-inverting output,
- one of the outputs of the first latch portion being coupled to one of the inputs of the second latch portion, having opposite polarity,
- one of the outputs of the second latch portion being coupled to one of the inputs of the first latch portion having opposite polarity,
- a differential input signal being provided at one of the inputs of the first latch portion and to one of the inputs of the second latch portion having opposite polarity, respectively, and
- each of the latch portions comprising a control input, coupled to a respective control signal, which determines a threshold for the input signal such that if the input signal is larger than the threshold the output latch is in a HIGH logic state and in a LOW state if the signal is smaller than the threshold, respectively. In the differential implementation, it is possible to identify a track circuit, which is the first latch portion and a latch, which is the second latch portion. A threshold of the first latch portion and second latch portion is determined by the control signals. Hence a relatively good adaptation to supply voltage is realized. Another advantage of the differential implementation is that it uses identical parts as single ended implementation and therefore the cost of implementation is relatively low and the design process is reduced when compared with the known implementations.

The embodiments refer to implementations in CMOS technology but the inventive concept may be applied mutatis-mutandis to other technologies as e.g. GaAs, SiGe, etc. As a consequence the terminals gate, source and drain correspond to base, emitter and collector, respectively.

The above and other features and advantages of the invention will be apparent from the following description of the exemplary embodiments of the invention with reference to the accompanying drawings, in which:

Fig. 1 depicts a block diagram of a latch circuit adapted to single ended input signals, according to the invention;

Fig. 2 depicts a transistor-level implementation of the latch circuit adapted to single ended input signals, according to an embodiment of the invention;

Fig. 3 depicts a block diagram of a latch circuit adapted to differential input signals, according to the invention;

Fig. 4 depicts a transistor level of a first embodiment of a latch circuit adapted to differential input signals, according to the invention;

Fig. 5 depicts a transistor level of a second embodiment of a latch circuit adapted to differential input signals, according to the invention; and

Fig. 6 depicts a prior-art latch circuit.

Fig. 1 depicts a block diagram of a latch circuit adapted to single ended input signals, according to the invention. The circuit comprises a differential input with an inverting input D+ and a non-inverting input D-. It is also provided a differential output with an inverting output Q+ and a non-inverting output Q- and a differential clock input with an inverting clock input Ck+ and a non-inverting clock input Ck-.

The non-inverting output Q- is coupled to the inverting input D+ and the non-inverting input D- is provided for receiving a single ended input signal In, which is memorized in the latch. The latch further comprises a control input for receiving a control signal V_{CM} for determining a threshold for the input signal In such that if the signal is at larger than the threshold the output latch is in a HIGH logic state and in a LOW state otherwise. Logical states of a logic circuit as a latch are determined inter alia by the supply voltage. It is defined a threshold level, which may be a current or a voltage, and a signal having an higher amplitude that the threshold level determines a logical 1 signal and a logical 0, otherwise. For a given family of logic circuits, the threshold level is depends on the supply voltage. In order to adapt to a relatively large set of supply voltages i.e. between 3V and .9 V, a control signal, which determines the threshold level is provided. Furthermore, the latch circuit is adapted to receive single ended signals and provides differential output signals.

This principle is further described with reference to Fig. 2 depicting a transistor-level implementation of the latch circuit adapted to single ended input signals, according to an embodiment of the invention. The circuit comprises a first pair of transistors with a first transistor M1 and a second transistor M3 having their sources coupled to each

other and a second pair of transistors comprising a third transistor M4 and a fourth transistor M5 having their sources coupled to each other. A gate of the second transistor M3 is coupled to a gate of the third transistor M4 and further coupled to the control signal VCM. It is provided a positive feedback from the non-inverting output Q- to a gate of the first transistor M1. The circuit further includes a pair of switches comprising a first switch M2 and a second switch M6 having their respective drains and sources coupled to the respective drains an sources of the first transistor M1 and the fourth transistor M5, respectively. Gate of the first switch M2 is driven by the inverting clock signal Ck+ and gate of the second switch (M5) is driven by the non-inverting clock signal Ck-. In the latch circuit shown in Fig. 2 the sources of the first transistor M1 and the second transistor M3 are supplied by a first current source I0 and the sources of the third transistor M4 and the fourth transistor M5 are supplied by a second current source I1. In a preferred embodiment, the first current source (I0) and the second current source I1 provide substantially equal currents and therefore the transistors M1, M2, M3 and M4, M5, M6 share the same current.In the latch circuit the drain of the first transistor M1 and the drain of the fourth transistor M5 are coupled to each other and further coupled to a supply voltage VDD via a first resistor R1. The drain of the second transistor M3 is coupled to a drain of the third transistor M4, the drains being further coupled to the supply voltage VDD via a second resistor R2. Optionally, the first resistor and the second resistor may have substantially identical values. The second resistor R2 is coupled to a reference terminal GND via a third current source I2. It should be observed that the current sources might be implemented in various ways as e.g. simply resistors, but for increase the overall performance of the latch versus temperature the first current source I0 and the second current source I1 comprise a series connection of a main current channel of a current source M13, M14, M15, M16 and a third resistor R3, as shown in Fig. 5. A voltage VC controls the controlled sources M13, M14, M15, M16. When temperature changes the resistance of the third resistor R3 resistor changes and therefore the source currents in the latch stages are adjusted accordingly in order to ensure a correct operation in a large temperature range.

In a tracking-mode, the inverting clock CK+ is considered to be HIGH, the non-inverting clock Ck- is considered to be LOW and the transistors M4 and M5 act as a differential pair sharing the current Io whereas M6 is in cut-off i.e. a negligible current circulates through it. The signal received at the non-inverting input D- is amplified at the inverting output Q+ and non-inverting output Q-. Accordingly, the transistor M2 gets the whole current Io forcing in cut-off the transistors M1 and M3. The condition is that the amplitude of the clock is sufficiently high to avoid any leak current from M1 and M3. The

voltage VCM provides a threshold for the input data in tracking mode and for the latch in the latching mode.

In a latching mode, the non-inverting clock CK- is asserted LOW, the inverted clock Ck+ is asserted HIGH and the transistor M6 takes the whole current I1. As a consequence, the transistors M4 and M5 are in cut-off . The transistor M2 is also in cut-off and the transistors M1 and M3 are active and the data is transferred from the input to the output and it is memorised.. This is a relatively fast circuit since the amplifying loop comprises a source follower M1 and a cascode transistor M3, having a relatively large bandwidth.

Table 1 shows the switching table of the latch with the analog values presented at the two outputs. The current source at the output I2 has the role of generating a differential operation with a swing of RI_0, where I_0=I1=I0.

D+	CK+	Q+[n]	Q+[n+1]	Q-[n+1]
0	0	0	V_{DD}-2RI_0	V_{DD}-RI_0
0	0	1	V_{DD}-RI_0	V_{DD}-2RI_0
0	1	0	V_{DD}-2RI_0	V_{DD}-RI_0
0	1	1	V_{DD}-2RI_0	V_{DD}-RI_0
1	0	0	V_{DD}-2RI_0	V_{DD}-RI_0
1	0	1	V_{DD}-RI_0	V_{DD}-2RI_0
1	1	0	V_{DD}-RI_0	V_{DD}-2RI_0
1	1	1	V_{DD}-RI_0	V_{DD}-2RI_0

Table 1

In Table 1 it was considered that all current sources deliver the same current I0. Furthermore, all resistors R1, R2 and R3 were considered equal to each other.

Since the input is not a differential input we can extend the basic circuit to a differential input, differential output circuit with some extra advantages compared to the simple basic idea as shown in Figs. 3 and 4.

Fig. 3 depicts a block diagram of a latch circuit adapted to differential input signals, according to the invention. The latch circuit is adapted for differential input signals In+, In- and comprises a first latch portion 1' and second latch portion 1'', which are substantially identical. Each latch portion comprises a differential input with an inverting input D1+, D2+ and a non-inverting input D1-, D2-, a differential output with an inverting output Q1+, Q2+ and a non-inverting output Q1-, Q2- and a differential clock input with an inverting clock input Ck1+, Ck2+ and a non-inverting clock input Ck1-, Ck2-. The inverting

clock inputs are coupled to each other and are further coupled to an inverting clock signal Ck+ and the non-inverting clock inputs being coupled to each other and being further coupled to a non-inverting clock signal Ck-. The non-inverting output Q1- of the first latch portion 1' is coupled to the inverting input (D2+) of the second latch portion (1"). The inverting output Q2+ of the second latch portion being coupled to the non-inverting input of the first latch portion D1-. A differential input signal In+, In- is provided at the non-inverting input of the first latch portion 1' and to the inverting input of the second latch portion 1", respectively, and each of the latch portions comprising a control input V_{CM1}, V_{CM2}, which is coupled a respective control signal V_{CM1}, V_{CM2}, which determines a threshold for the input signal In+, In- such that if the signal is at larger than the threshold the output latch is in a HIGH logic state and in a LOW state, otherwise. In the differential implementation, it is possible to identify a track circuit, which is the first latch portion 1' and a latch, which is the second latch portion 1". A threshold of the first latch portion 1' and second latch portion 1" is determined by the control signals V_{CM1}, V_{CM2}. Hence, a relatively good adaptation to supply voltage VDD is of the threshold voltages of the latch circuit is realized. Another advantage of the differential implementation is that it uses identical parts as single ended implementation and therefore the cost of implementation is relatively low and the design process is reduced when compared with the known implementations.

Fig. 4 depicts a transistor level of a first embodiment of a latch circuit adapted to differential input signals, according to the invention. The latch circuit comprises transistors, each transistor comprising a source, a gate and a drain, and wherein each latch portion 1'; 1" comprises a first pair of transistors comprising a first transistor M1A; M1B and a second transistor M3A; M3B, having their sources coupled each other, respectively. The latch circuit further comprises a second pair of transistors comprising a third transistor M4A; M4B and a fourth transistor M5A; M5B, having their sources coupled each other, respectively. A gate of the second transistor M3A; M3B is coupled to a gate of the third transistor M4A; M4B respectively and further coupled to a DC voltage level VCM. In this particular implementation it was considered that the control signals V_{CM1}, V_{CM2} are equal to each other and further equal to V_{CM}. A pair of switches comprising a first switch M2A; M2B and a second switch M6A; M6B, the switches including transistors having their respective drains and sources coupled to the respective drains an sources of the first transistor M1A; M1B and the fourth transistor M5A; M5B, respectively, is also provided. The gate of the first switch M2A; M2B is driven by a binary clock signal Ck- and gate of the second switch M6A; M6B being driven by an inverted binary clock signal Ck+. The two latch portions 1', 1" are

crossed-coupled such that a gate of the first transistor M1A; M1B of a portion is coupled to the respective output of the other portion INTQ-; INTQ+, respectively.

The sources of the first transistor M1A, M1B and the second transistor M3A, M3B are supplied by a first current source I0. The sources of the third transistor M4A, M4B and the fourth transistor M5A, M5B are supplied by a second current source I1. Particularly, the current sources deliver substantially equal currents.

The drain of the first transistor M1A; M1B and the drain of the fourth transistor M5A; M5B are coupled to each other respectively and further coupled to a supply voltage VDD via a resistor R1. The drain of the second transistor M3A; M3B is coupled to a drain of the third transistor M4A; M4B, respectively, the drains being further coupled to the supply voltage VDD via a second resistor R2.

In the tracking-mode, the non-inverting clock CK- is HIGH asserted, and consequently the inverting clock Ck+ is LOW asserted, and the D+, D- input voltages are amplified at the internal nodes INTQ- and INTQ+ and Q+, Q- respectively. Since M5 and M8 are conducting, the latch is in cut-off and no latching action is possible. In the latching mode, the non-inverting clock CK- is HIGH asserted, and consequently the inverting clock CV is LOW asserted. The transistors M2 and M11 are cut-off now. The information from the D+, D- inputs is not passed at the outputs. The transistors M6 and M7 are active now and the information present at the internal nodes A and B is latched. Regarding Fig. 4 it is observed that data has two paths: a path to the output via the common-source, common-gate configurations M2,M3 and M11, M10 respectively and a path to the internal nodes INTQ- and INTQ+ via common source transistors M2 and M11. Hence, the latch and the gain stages may be optimized separately ensuring different loads for the latch R1 and the output R2. Moreover, when the latch is taking decisions at the outputs A and B the transistors M4 and M9 are active and the information present at the nodes A and B is amplified at the outputs Q+, Q- with a high speed provided by the paraphase stages M6, M4 and M7, M9. This determines a reduction of setup and hold times.

Fig. 5 depicts a transistor level of a second embodiment of a latch circuit adapted to differential input signals, according to the invention. The first current source I0 and the second current source I1 comprises a series connection of a main current channel of a controlled current source M13, M14, M15, M16 and a third resistor R3. A voltage VC controls the controlled sources M13, M14, M15, M16. It should be observed that the current sources might be implemented in various ways as e.g. simply resistors, but for increase the overall performance of the latch versus temperature the first current source I0 and the second

current source I1 comprise a series connection of a main current channel of a current source M13, M14, M15, M16 and a third resistor R3. A voltage VC controls the controlled sources M13, M14, M15, M16. When temperature changes the resistance of the third resistor R3 resistor changes and therefore the source currents in the latch stages are adjusted accordingly in order to ensure a correct operation in a large temperature range.

It is remarked that the scope of protection of the invention is not restricted to the embodiments described herein. Neither is the scope of protection of the invention restricted by the reference numerals in the claims. The word 'comprising' does not exclude other parts than those mentioned in the claims. The word 'a(n)' preceding an element does not exclude a plurality of those elements. Means forming part of the invention may both be implemented in the form of dedicated hardware or in the form of a programmed purpose processor. The invention resides in each new feature or combination of features.

CLAIMS:

1. A latch circuit (1) comprising,

- a differential input with an inverting input (D+) and a non-inverting input (D-),
- a differential output with an inverting output (Q+) and a non-inverting output (Q-),
- one of the outputs (Q-) being coupled to one of the inputs input (D+) having an opposite polarity,
- a control input for receiving a control signal (V_{CM}) for determining a threshold for an input signal (In) such that if the input signal is at larger than the threshold the non-inverting output s in a HIGH logic state and in a LOW state if the input signal is smaller than the threshold, respectively.

2. A latch circuit as claimed in claim 1 comprising transistors, each transistor comprising a source, a gate and a drain, the latch further comprising,

- a first pair of transistors comprising a first transistor (M1) and a second transistor (M3) having their sources coupled to each other,
- a second pair of transistors comprising a third transistor (M4) and a fourth transistor (M5) having their sources coupled to each other,
- a gate of the second transistor (M3) being coupled to a gate of the third transistor (M4) and further coupled to the control signal (VCM),
- a positive feedback from the non-inverting output (Q-) to a gate of the first transistor (M1),
- a pair of switches comprising a first switch (M2) and a second switch (M6) having their respective drains and sources coupled to the respective drains an sources of the first transistor (M1) and the fourth transistor (M5), respectively, and
- gate of the first switch (M2) being driven by the inverting clock signal (Ck+) and gate of the second switch (M5) being driven by the non-inverting clock signal (Ck-).

3. A latch as claimed in claim 2, wherein

- the sources of the first transistor (M1) and the second transistor (M3) are supplied by a first current source (I0),
- the sources of the third transistor (M4) and the fourth transistor (M5) are supplied by a second current source (I1).

4. A latch circuit as claimed in claim 3, wherein the first current source (I0) and the second current source (I1) provide substantially equal currents.

5. A latch circuit as claimed in one of the claims 2 to 4, wherein the drain of the first transistor (M1) and the drain of the fourth transistor (M5) are coupled to each other and further coupled to a supply voltage (VDD) via a first resistor means (R1).

6. A latch circuit as claimed one of the claims 2 to 5, wherein the drain of the second transistor (M3) is coupled to a drain of the third transistor (M4), the drains being further coupled to the supply voltage (VDD) via a second resistor means (R2).

7. A latch circuit as claimed in one of the claims 2 to 7, wherein the second resistor means is coupled to a reference terminal (GND) via a third current source (I2).

8. A latch circuit as claimed in any of the preceding claims, wherein the first current source (I0) and the second current source (I1) comprises a series connection of a main current channel of a current source (M13, M14, M15, M16) and a third resistor means (R3).

9. A latch circuit as claimed in claim 8, wherein the controlled sources (M13, M14, M15, M16) are controlled by a voltage (VC).

10. A latch circuit as claimed in claim 1, adapted for differential input signals (In+, In-) and comprising a first latch portion (1') and second latch portion (1''), which are substantially identical, each latch portion comprising

- a differential input with an inverting input (D1+, D2+) and a non-inverting input (D1-, D2-),
- a differential output with an inverting output (Q1+, Q2+) and a non-inverting output (Q1-, Q2-),

- one of the outputs (Q1-) of the first latch portion (1') being coupled to one of the inputs (D2+) having opposite polarity of the second latch portion (1"),
- one of the outputs (Q2+) of the second latch portion being coupled to one of the inputs having opposite polarity of the first latch portion (D1-),
- a differential input signal (In+, In-) being provided at one of the inputs of the first latch portion (1') and to one of the inputs having an opposite polarity of the second latch portion (1"), respectively, and
- each of the latch portions comprising a control input (V_{CM1}, V_{CM2}), which is coupled a respective control signal (V_{CM1}, V_{CM2}), which determines a threshold for the input signal (In+, In-) such that if the input signal is at larger than the threshold the output latch is in a HIGH logic state and in a LOW state if the signal is smaller than the threshold, respectively.

11. A latch circuit as claimed in claim 10 comprising transistors, each transistor comprising a source, a gate and a drain, and wherein each latch portion (1'; 1") comprises
- a first pair of transistors comprising a first transistor (M1A; M1B) and a second transistor (M3A; M3B), having their sources coupled each other, respectively
- a second pair of transistors comprising a third transistor (M4A; M4B) and a fourth transistor (M5A; M5B), having their sources coupled each other, respectively
- a gate of the second transistor (M3A; M3B) being coupled to a gate of the third transistor (M4A; M4B) respectively and further coupled to a DC voltage level (VCM),
- a pair of switches comprising a first switch (M2A; M2B) and a second switch (M6A; M6B), the switches including transistors having their respective drains and sources coupled to the respective drains an sources of the first transistor (M1A; M1B) and the fourth transistor (M5A; M5B), respectively,
- gate of the first switch (M2A; M2B) being driven by a binary clock signal (Ck+) and gate of the second switch (M6A; M6B) being driven by an inverted binary clock signal (Ck-), and
- the two latch portions (1', 1") being crossed-coupled such that a gate of the first transistor (M1A; M1B) of a portion is coupled to the respective output of the other portion (INTQ-; INTQ+), respectively.

12. A latch as claimed in Claim 11 wherein

- the sources of the first transistor (M1A, M1B) and the second transistor (M3A, M3B) are supplied by a first current source (I0),
- the sources of the third transistor (M4A, M4B) and the fourth transistor (M5A, M5B) are supplied by a second current source (I1).

13. A latch circuit as claimed in claim 12, wherein the first current source (I0) and the second current source (I1) provide substantially equal currents.

14. A latch circuit as claimed in one of the claims 10 to 13, wherein the drain of the first transistor (M1A; M1B) and the drain of the fourth transistor (M5A; M5B) are coupled to each other respectively and further coupled to a supply voltage (VDD) via a first resistor means (R1).

15. A latch circuit as claimed in one of the claims 10 to 14, wherein the drain of the second transistor (M3A; M3B) is coupled to a drain of the third transistor (M4A; M4B), respectively the drains being further coupled to the supply voltage (VDD) via a second resistor means (R2).

16. A latch circuit as claimed in one of the claims 10 – 15, wherein the first current source (I0) and the second current source (I1) comprises a series connection of a main current channel of a controlled current source (M13, M14, M15, M16) and a third resistor means (R3).

17. A latch circuit as claimed in claim 16, wherein the controlled sources (M13, M14, M15, M16) are controlled by a voltage (VC).

ABSTRACT:

A latch circuit (1) comprising, a differential input with an inverting input (D+) and a non-inverting input (D-). The latch further comprises a differential output with an inverting output (Q+) and a non-inverting output (Q-). One of the outputs (Q-) is coupled to one of the inputs input (D+) having an opposite polarity. The latch further comprises a control input for receiving a control signal (V_{CM}) for determining a threshold for an input signal (In) such that if the input signal is at larger than the threshold the non-inverting output s in a HIGH logic state and in a LOW state if the input signal is smaller than the threshold, respectively.

Fig. 1

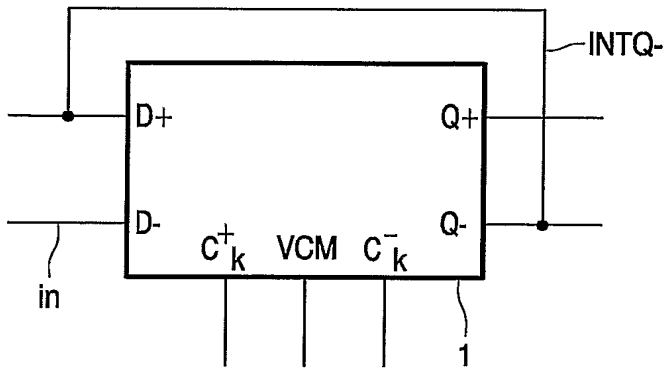
INTQ-
D+
Q+
D-
Q-
C_k^+
VCM
C_k^-
in
1

FIG. 1

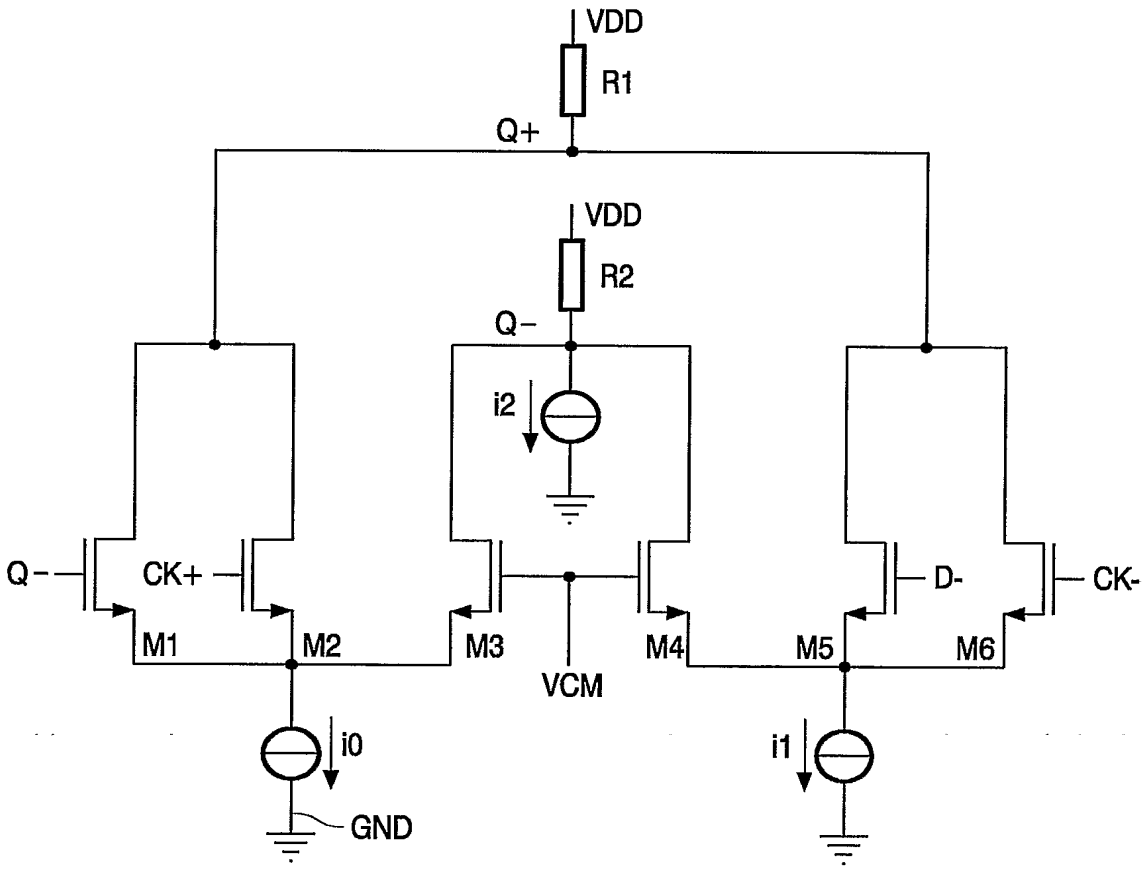
VDD
R1
Q+
VDD
R2
Q−
i2
Q−
CK+
D-
CK-
M1
M2
M3
M4
M5
M6
VCM
i0
i1
GND

FIG. 2

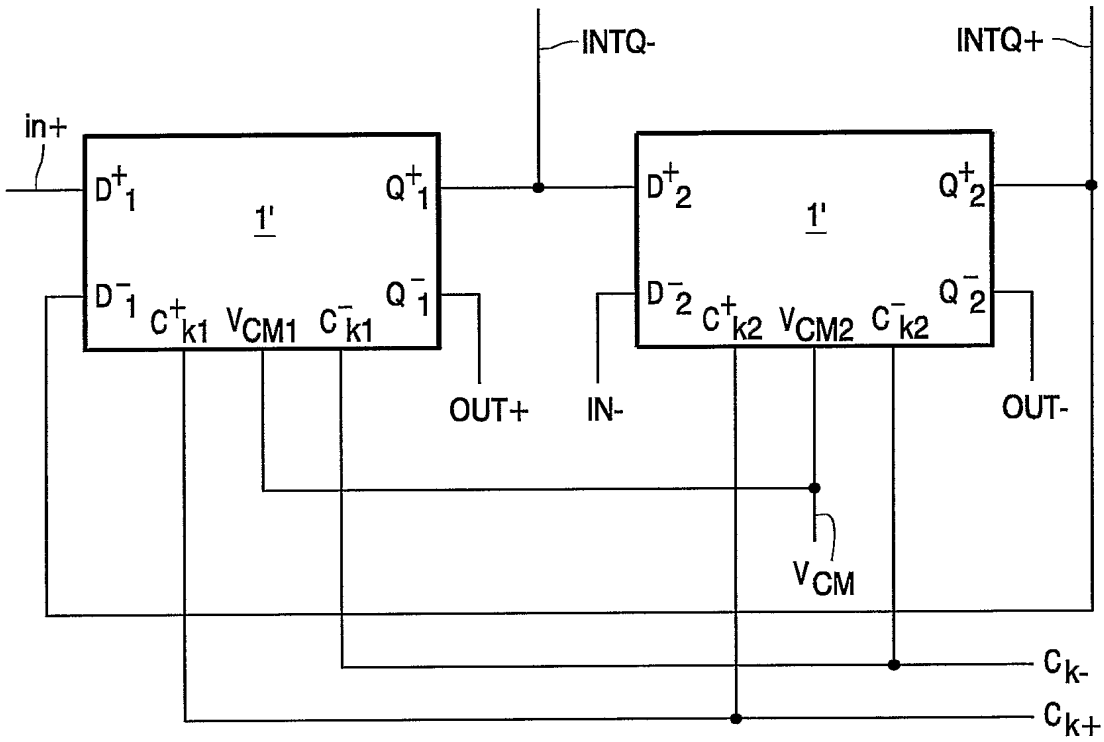
INTQ-
INTQ+
in+
D+1
Q+1
1'
D−1
C+k1
VCM1
C−k1
Q−1
D+2
Q+2
1'
D−2
C+k2
VCM2
C−k2
Q−2
OUT+
IN-
OUT-
VCM
Ck-
Ck+

FIG. 3

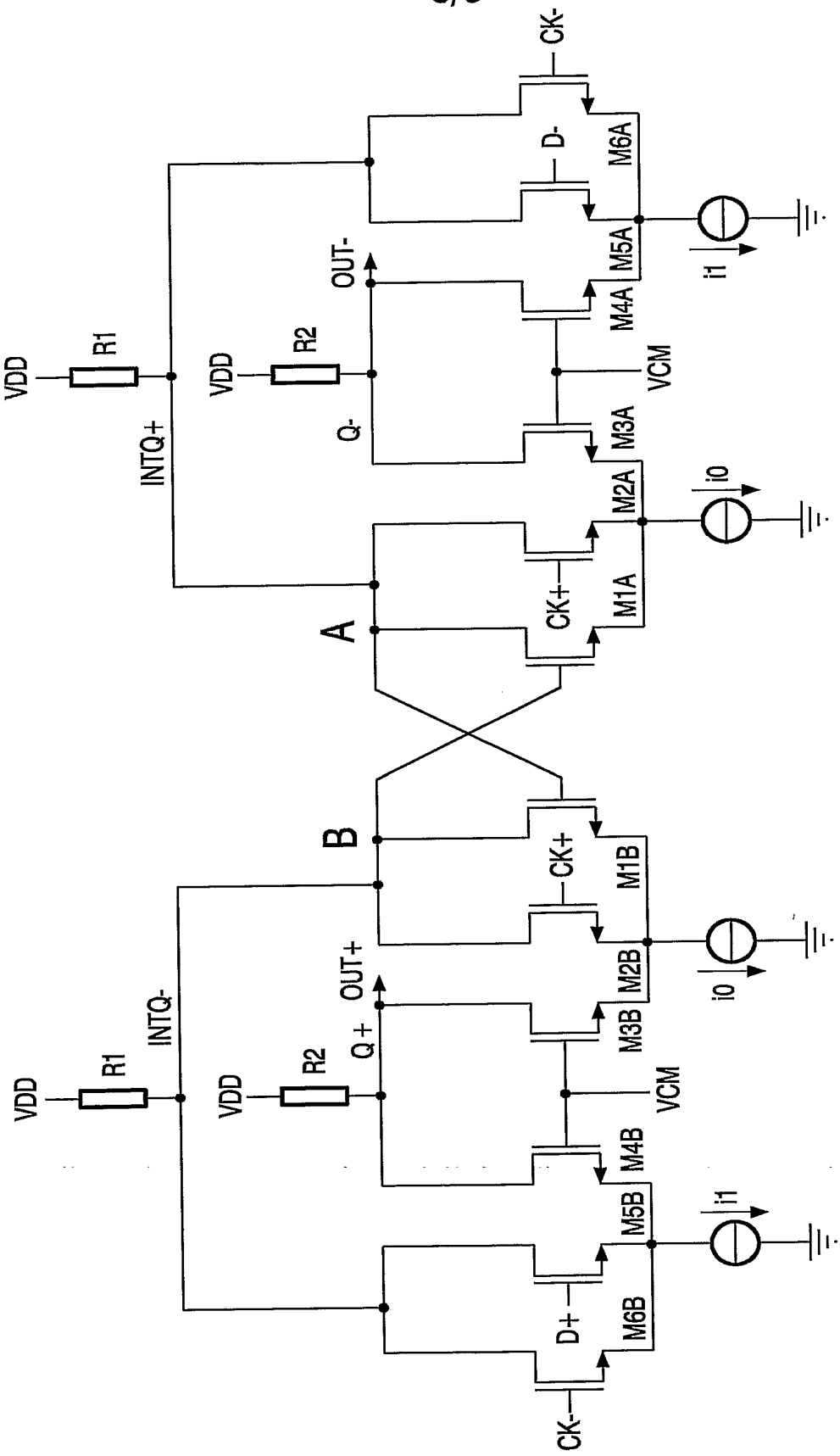
VDD
R1
INTQ+
VDD
R2
OUT-
Q-
CK-
D-
M6A
M5A
M4A
VCM
M3A
M2A
M1A
CK+
i1
i0
A
B
VDD
R1
INTQ-
VDD
R2
OUT+
Q+
CK+
M1B
M2B
M3B
VCM
M4B
M5B
M6B
D+
CK-
i0
i1

FIG. 4

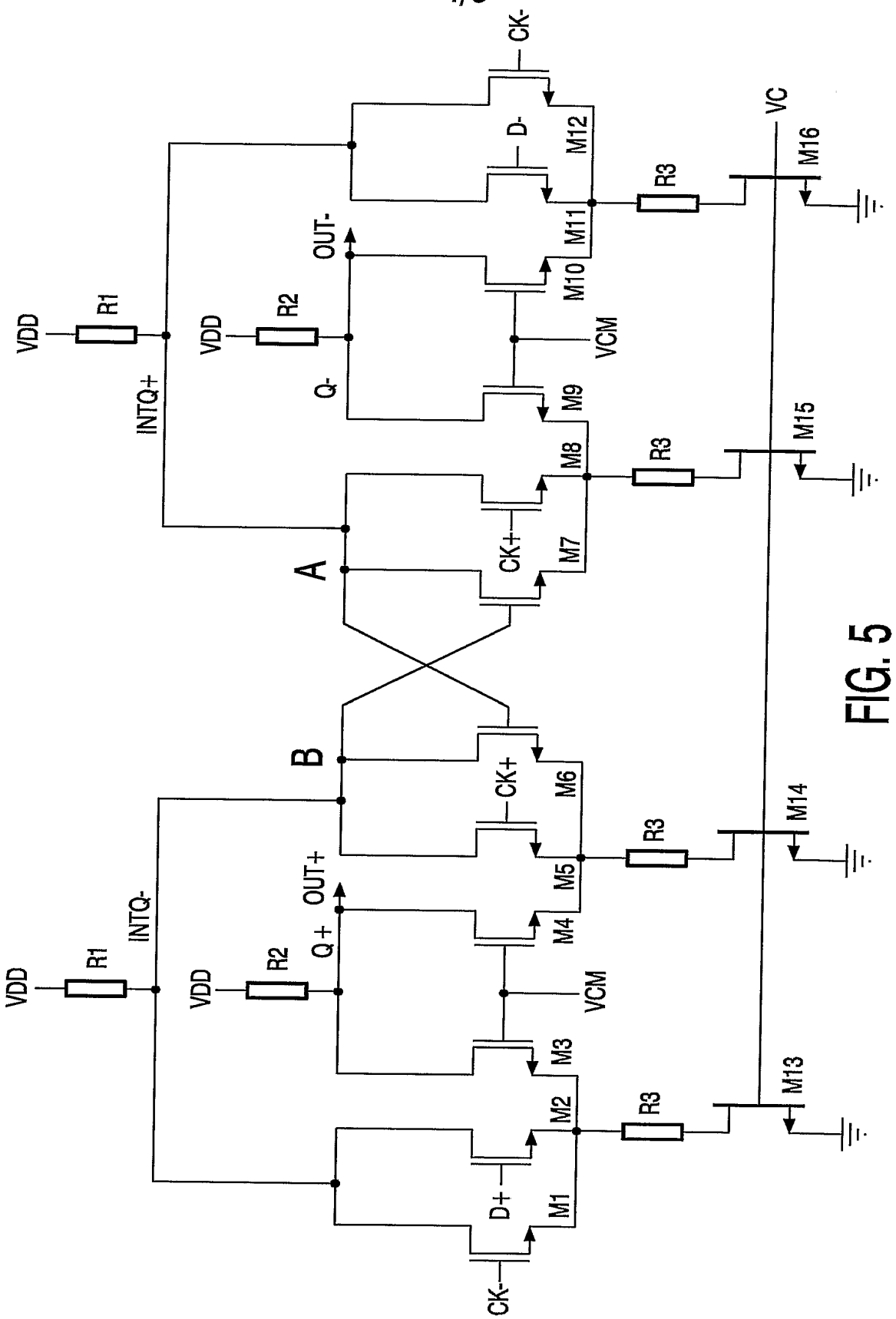
CK-
D-
M12
VC
M16
R3
OUT-
M11
M10
VDD
R1
VDD
R2
VCM
INTQ+
Q-
M9
M8
R3
M15
A
CK+
M7
B
CK+
M6
R3
M14
OUT+
M5
INTQ-
Q+
M4
VDD
R1
VDD
R2
VCM
M3
M2
R3
M13
D+
M1
CK-

FIG. 5

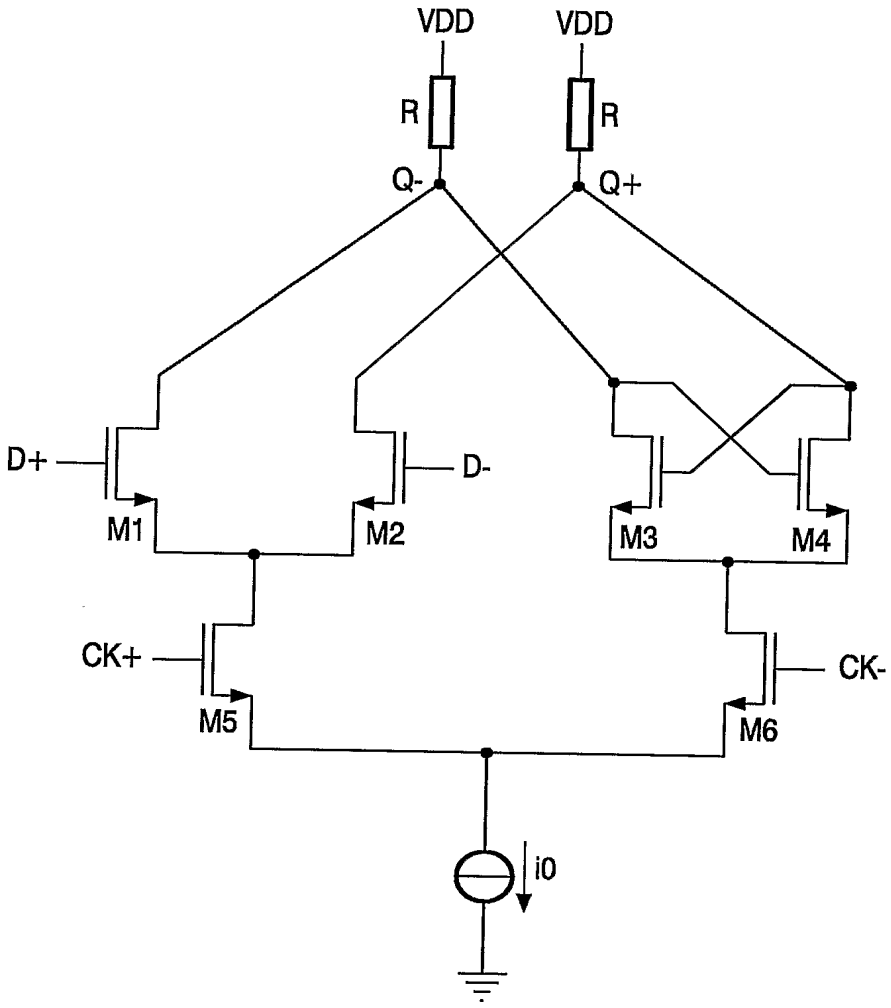

FIG. 6

PCT/IB2005/050286